WHAT IS CLAIMED IS:

1. A method for hermetically sealing devices, the method comprising:

providing a substrate, the substrate including a plurality of individual chips, each of the chips including a plurality of devices, each of the chips being arranged in a spatial manner as a first array, the array configuration including a plurality of first street regions arranged in strips and a plurality of second street regions arranged in strips, the second street regions intersecting the first street regions to form the array configuration;

providing a transparent member of a predetermined thickness, the transparent member including a plurality of recessed regions within the predetermined thickness and arranged in a spatial manner as a second array, each of the recessed regions being bordered by a standoff region, the standoff region having a thickness defined by a portion of the predetermined thickness;

aligning the transparent member in a manner to couple each of the plurality of recessed regions to a respective one of said plurality of chips whereupon the standoff region being coupled to each of the plurality of first street regions and being coupled to each of the plurality of second street regions to enclose each of the chips within one of the respective recessed regions; and

hermetically sealing each of the chips within one of the respective recessed regions by contacting the standoff region of the transparent member to the plurality of first street regions and second street regions using at least a bonding process to isolate each of the chips within one of the recessed regions.

2. The method of claim 1 wherein each of the first street regions has a first width ranging from about 0.5 mm to 1.0 mm in dimension and each of the second street regions has a second width ranging from about 0.5 mm to 1.0 mm in dimension.

3. The method of claim 1 wherein the transparent member has an optical power transmittance of greater than about 99%.

4. The method of claim 1 wherein the transparent member is characterized by a coefficient of thermal expansion α_T, the coefficient of thermal expansion is about the same as a coefficient of thermal expansion α_S of the substrate.

5. The method of claim 1 wherein the transparent member comprises an antireflective coating disposed overlying surface regions of each of the recessed regions.

6. The method of claim 1 wherein each of the recessed regions is formed by a process selected from dry or wet etching, laser machining, acoustic machining, and casting.

7. The method of claim 1 wherein the transparent member comprises a first transparent member overlying a standoff layer, the standoff layer including the standoff region.

8. The method of claim 1 wherein the standoff layer comprises a second transparent member.

9. The method of claim 1 wherein the bonding process is selected from at least a plasma activated bonding, eutectic bonding, glue layer or adhesive bonding, welding, anodic bonding, and fusion bonding.

10. The method of claim 1 wherein the transparent member is characterized by a thickness ranging from about 0.1 mm to 1.2 mm.

11. The method of claim 1 wherein each of the chips is maintained within an inert environment within one of the respective recessed regions.

12. The method of claim 11 wherein the inert environment is selected from nitrogen, argon, or a mixture of nitrogen and argon.

13. The method of claim 12 wherein the inert environment causes a damping process.

14. The method of claim 12 wherein the inert environment causes a reduction in electrical breakdown.

15. The method of claim 1 wherein each of the chips comprises an interconnect region, the interconnect region being outside of the recessed region.

16. The method of claim 15 wherein the interconnect region is exposed through a through hole region on the transparent member.

17. The method of claim 16 wherein the interconnect region comprises a plurality of bonding pads.

18. The method of claim 1 wherein the substrate comprises a silicon bearing material.

19. The method of claim 18 wherein the substrate is a silicon wafer.

20. The method of claim 1 wherein each of the recessed regions comprises a first surface region coupled to a second surface region, the first surface region and the second surface region characterized to be of optical quality.

21. The method of claim 20 wherein the first surface region has a root mean square surface roughness of less than or equal to 2 Å for a 2 μm by 2 μm area.

22. The method of claim 1 wherein each of the recessed regions is annular in shape.

23. The method of claim 1 wherein each of the recess regions has a depth of about 0.5 mm and less.

24. The method of claim 1 wherein the transparent member comprises a first side and a second side, the first side being parallel to the second side, the first side and the second side being coated with an antireflective material.

25. The method of claim 24 wherein the coating of antireflective material reduces the reflectance of visible light at the first side and the second side to less than 2% per side.

26. The method of claim 24 wherein the antireflective material comprises MgF_2.

27. The method of claim 1 further comprising:

dicing at least one of the chips by scribing a portion of each of the first street regions and by scribing a portion of each of the second street regions;

attaching at least one of the chips within one of the respective recessed regions to a lead frame structure;

wire bonding a portion of the attached chip to a portion of the lead frame structure; and

encapsulating the wire bonded portion of the attached chip and the portion of the lead frame structure while maintaining a surface region of the transparent substrate defined on the recessed region free of encapsulant.

28. The method of claim 1 wherein each of the recessed regions has a peripheral region that filters out light.

29. The method of claim 1 wherein each of the recessed regions has a peripheral region that forms an aperture region overlying a portion of one of the respective chips.

30. The method of claim 1 wherein at least one of the plurality of devices comprises a plurality of charge coupled devices, a plurality of deflection devices, a plurality of sensing devices, and an integrated circuit device.

31. A system for hermetically sealing devices, the system comprising:

a substrate, the substrate configured to include a plurality of individual chips, wherein each of the chips includes a plurality of devices;

wherein each of the chips are arranged in a spatial manner as a first array, the array configuration including a plurality of first street regions arranged in strips and a plurality of second street regions arranged in strips, the second street regions intersecting the first street regions to form the array configuration;

a transparent member of a predetermined thickness, the transparent member configured to include a plurality of recessed regions within the predetermined thickness, wherein the plurality of recessed regions are arranged in a spatial manner as a second array, and wherein each of the recessed regions are bordered by a standoff region having a thickness defined by a portion of the predetermined thickness;

wherein the substrate and the transparent member are aligned in a manner to couple each of the plurality of recessed regions to a respective one of said plurality of chips, whereupon the standoff region is coupled to each of the plurality of first street regions and is coupled to each of the plurality of second street regions to enclose each of the chips within one of the respective recessed regions; and

wherein each of the chips within one of the respective recessed regions is hermetically sealed by contacting the standoff region of the transparent member to the

plurality of first street regions and second street regions using at least a bonding process to isolate each of the chips within one of the recessed regions.

32. The system of claim 31 wherein each of the first street regions has a first width ranging from about 0.5 mm to 1.0 mm in dimension and each of the second street regions has a second width ranging from about 0.5 mm to 1.0 mm in dimension.

33. The system of claim 31 wherein the transparent member has an optical power transmittance of greater than about 99%.

34. The system of claim 31 wherein the transparent member is characterized by a coefficient of thermal expansion α_T, the coefficient of thermal expansion is about the same as a coefficient of thermal expansion α_S of the substrate.

35. The system of claim 31 wherein the transparent member comprises an antireflective coating disposed overlying surface regions of each of the recessed regions.

36. The system of claim 31 wherein each of the recessed regions is formed by a process selected from dry or wet etching, laser machining, acoustic machining, and casting.

37. The system of claim 31 wherein the transparent member comprises a first transparent member overlying a standoff layer, the standoff layer including the standoff region.

38. The system of claim 31 wherein the standoff layer comprises a second transparent member.

39. The system of claim 31 wherein the bonding process is selected from at least a plasma activated bonding, eutectic bonding, glue layer or adhesive bonding, welding, anodic bonding, and fusion bonding.

40. The system of claim 31 wherein the transparent member is characterized by a thickness ranging from about 0.1 mm to 1.2 mm.

41. The system of claim 31 wherein each of the chips is maintained within an inert environment within one of the respective recessed regions.

42. The system of claim 41 wherein the inert environment is selected from nitrogen, argon, or a mixture of nitrogen and argon.

43. The system of claim 42 wherein the inert environment causes a damping process.

44. The system of claim 42 wherein the inert environment causes a reduction in electrical breakdown.

45. The system of claim 31 wherein each of the chips comprises an interconnect region, the interconnect region being outside of the recessed region.

46. The system of claim 45 wherein the interconnect region is exposed through a through hole region on the transparent member.

47. The system of claim 46 wherein the interconnect region comprises a plurality of bonding pads.

48. The system of claim 31 wherein the substrate comprises a silicon bearing material.

49. The system of claim 48 wherein the substrate is a silicon wafer.

50. The system of claim 31 wherein each of the recessed regions comprises a first surface region coupled to a second surface region, the first surface region and the second surface region characterized to be of optical quality.

51. The system of claim 50 wherein the first surface region has a root mean square surface roughness of less than or equal to 2 Å for a 2 μm by 2 μm area.

52. The system of claim 31 wherein each of the recessed regions is annular in shape.

53. The system of claim 31 wherein each of the recess regions has a depth of about 0.5 mm and less.

54. The system of claim 31 wherein the transparent member comprises a first side and a second side, the first side being parallel to the second side, the first side and the second side being coated with an antireflective material.

55. The system of claim 54 wherein the coating of antireflective material reduces the reflectance of visible light at the first side and the second side to less than 2% per side.

56. The system of claim 54 wherein the antireflective material comprises MgF_2.

57. The system of claim 31 further comprising:

a lead frame structure;

wherein at least one of the chips is diced by scribing a portion of each of the first street regions and by scribing a portion of each of the second street regions,

wherein at least one of the chips within one of the respective recessed regions is attached to the lead frame structure;

wherein a portion of the attached chip is wire bonded to a portion of the lead frame structure ; and

wherein the wire bonded portion of the attached chip and the portion of the lead frame structure is encapsulated while maintaining a surface region of the transparent substrate defined on the recessed region free of encapsulant.

58. The system of claim 31 wherein each of the recessed regions has a peripheral region that filters out light.

59. The system of claim 31 wherein each of the recessed regions has a peripheral region that forms an aperture region overlying a portion of one of the respective chips.

60. The system of claim 31wherein at least one of the plurality of devices comprises a plurality of charge coupled devices, a plurality of deflection devices, a plurality of sensing devices, and an integrated circuit device.